REMARKS

In accordance with the foregoing, claim 12 has been amended and claim 26 has been added. Claims 11-26 are pending and under consideration.

With regard to item 2 of the Office Action, claim 12 has been amended to address the objection raised by the Examiner.

In item 4 of the Office Action, claims 11-25 are rejected under 35 USC § 103(a) as being obvious over Bretthauer et al., BRASIL: The Braunschweig Mixed-Mode-Simulator for Integrated Circuits ("the Bretthauer paper") in view of the H. Spiro, Simulation of Integrated Circuits ("the Spiro paper").

In reviewing the application, an English language translation of the Spiro paper could not be located. Although the Spiro paper is described in the specification, it is believed that a translation is appropriate so that the record will reflect that the paper has been completely considered and that the claims patentably distinguish thereover. The undersigned is in the process of obtaining a translation. The translation will be forwarded to the Examiner upon receipt. In the meantime, if the Examiner's file already contains a translation, the undersigned would appreciate a telephone call indicating that an additional translation is unnecessary.

The Spiro paper discloses the charging method for simulating integrated circuits. See section 3.73 spanning pages 211 through 216. The Spiro paper does not disclose adding an additional element to each node of the circuit. Moreover, the Spiro paper does not disclose adding a chargeable dynamic element to each node of the circuit, as claimed. Instead, Spiro teaches to set capacitances and inductances in the network to be analyzed to unity. See equation 37.14 and the preceding paragraph on page 211 of the reference. No capacitances are added to each node of the circuit for calculation purposes.

The Bretthauer paper does not disclose adding an element to each node of the circuit for any purpose. The Bretthauer paper certainly does not suggest adding a chargeable dynamic element to each node of the circuit. As mentioned in the previous Office Action, the Bretthauer paper is clear that the simulation is not performed in this manner. The Examiner's attention is called to the sentence bridging pages 2 and 3 of the reference, which states "The capacitances are the sums of the parasitic capacitances of the transistors and all capacitances tied to a node." There is not even a hint for adding a chargeable dynamic element in a charging method for the parallel calculation of individual partitions of an electric circuit. Further, the Spiro paper does not suggest the use of an additional chargeable dynamic element at each node of the circuit in performing the charging method.

The Examiner specifically addresses adding a chargeable dynamic element in item 5, on page 3 of the Office Action. The Examiner states that the references disclose "providing a chargeable dynamic element at each node of the circuit (Bretthauer paper, § 4, wherein the capacitor is the chargeable dynamic element; Coupling of the simulation algorithms, column 2)." Section 4 has been carefully reviewed. Perhaps the Examiner has noted the sentence "The timing simulator performs a dynamic partitioning during the simulation," and the sentence "For the timing algorithms, the gates of MOS transistors in the area of the circuit simulation can be treated as constant capacitors."

Perhaps the Examiner believes that the circuit contains gates, not capacitors. Therefore, when the gates are treated as capacitors, a capacitor is added. However, the gates have a capacitance associated therewith. Even if the Examiner were correct that treating the gates as constant capacitors equals "adding a chargeable dynamic element," the claims still patentably distinguish over the references. Specifically, the independent claims require that a chargeable dynamic element be added to each node of the circuit. In the Bretthauer paper, certainly there are nodes of the circuit other than the nodes associated with gates of MOS transistors.

For all of the above reasons, it is submitted that the obviousness rejection should be withdrawn. There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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